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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,305	10/27/2000	Takaki Yoshida	YMOR:186	4222

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PARKHURST & WENDEL, LLP
1421 Prince Street, Suite 210
Alexandria, VA 22314

EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	7

DATE MAILED: 05/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,305	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *23-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, Claims 1-22, in Paper No. 6 is acknowledged. The traversal is on the ground(s) that claims 1-52 is sufficiently related that a thorough and complete search for the subject matter of the elected claims would necessarily encompass a thorough and complete search for the subject matter of the non-elected claims. This is not found persuasive because Layout and Masking occurs before a semiconductor circuit is operable and hence, during layout and masking a semiconductor circuit is not even operable for testing. Since Group I, Claims 1-22, is directed to testing and Group II is directed to Layout and Masking, the two inventions are not even related. Furthermore; it has been deemed by the US Patent and Trademark office that Group I, Claims 1-22 would be most appropriately examined by an Examiner in Art Unit 2133 and Group II, Claims 23-52 would be most appropriately examined by an Examiner in Art Unit 2825.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Goel, Prabhakar (US 4204633 A).

35 U.S.C. 102(b) rejection of claims 1 and 12.

Goel teaches a fault detecting method for a semiconductor integrated circuit (see Figure 1 and col. 2, lines 36-65 in Goel; Note: Goel teaches a method whereby a set of faults and a pattern generator are used in a method whereby chips are tested for faults), characterized in that: a fault list corresponding to information on sites of a semiconductor integrated circuit where a fault is likely to occur or information required to reduce faults is used to perform detection for faults in said semiconductor integrated circuit (col. 6, line 3-5 of Goel teach that each selected fault from the fault list is a fault associated with a specific node of the combinational or sequential circuit logic network).

35 U.S.C. 102(b) rejection of claims 2 and 13.

Goel teaches faults that are difficult to detect are omitted from the fault list before detection is performed for faults in the semiconductor integrated circuit using a remaining part of the fault list (col. 2, lines 66-68, Goel teaches that faults which occur at a frequency below a predetermined level are eliminated from the set of faults; Note: faults which occur at a frequency below a predetermined level are faults that are difficult to detect due to the lack of frequency of occurrence).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 3, 5, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goel, Prabhakar (US 4204633 A) in view of Hori, Satoshi et al. (US 5587930 A, hereafter referred to as Hori).

35 U.S.C. 103(a) rejection of claims 3 and 14.

Goel, substantially teaches the claimed invention described in claims 1 and 2 (as rejected above).

However Goel, does not explicitly teach the specific use of a fault list containing data on **likelihood** of each fault.

Hori, in an analogous art, teaches a fault list in the form of a fault tree containing data on **likelihood** of each fault (see Abstract, Hori). The Examiner asserts that that Goel

teaches that faults in the fault list are processed one at a time as faults are selected from the fault list (col. 2, lines 50-53, Goel) and that difficult to detect faults, i.e., faults with a lower probability of occurrence, are eliminated from the fault list (col. 2, lines 66-68, Goel), hence the Goel patent requires statistical information on the probability of occurrence for faults in order to determine which faults should be eliminated. Hori provides a required element of the Goel patent by including probability information for faults in a fault tree list.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Goel with the teachings of Hori by including use of a fault list containing data on **likelihood** of each fault. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a fault list containing data on **likelihood** of each fault would have provided the opportunity to eliminate faults falling below a given threshold for a given probability of occurrence (col. 2, lines 66-68, Goel).

35 U.S.C. 103(a) rejection of claims 5 and 16.

Note: Storing the likelihood data of a fault in the fault list with the fault is a means for weighting the fault with the likelihood data (see rejection to claim 3, above).

Allowable Subject Matter

4. Claims 4, 6-11, 15 and 17-22 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The present invention pertains to a fault detecting method for a semiconductor chip using a fault list with information on sites of a semiconductor integrated circuit where a fault is likely to occur. Claim 4 recites various features:

"wherein detection is performed for faults in the semiconductor integrated circuit using a fault list ordered with the likelihood of each fault".

The Prior Art of record teach fault detecting methods for a semiconductor chip using a fault list with information on sites of a semiconductor integrated circuit where a fault is likely to occur (see Prior Art rejections of claims 1-3, 5, 12-14 and 15, above). The prior art however specifically teach away from ordering the fault list according to likelihood since as taught in the Hori patent the fault tree list is ordered according to hardware requirements of the device and cannot be ordered according to likelihood. Hence the prior art taken alone or in any combination fail to teach the claimed novel feature in claim 4 in view of its base and intervening claims.

Claims 6, 15 and 17 cite similar language as in claim 4.

Claims 7-11 and 18-22 depend from respective claims 4, 6, 15 and 17.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bershteyn, Mikhail (US 5414716 A) teaches iteratively testing an integrated circuit with calculated weights from successively reduced lists of undetected faults by calculating additional weights directly from the reduced list of undetected faults from a previous iteration. Tamarapalli, Nagesh et al. (US 5737340 A) teaches a reduced list of undetected faults is determined through exact fault simulation. Giordano, Gerard J. et al. (US 5544308 A) teaches automated diagnosis of faults in a system containing repairable parts is performed by selecting a set of faults representing all known failures which can occur among the parts of the system. Ruiz, G.; Mitchell, J.; Buron, A.; Switch-level fault detection and diagnosis environment for MOS digital circuits using spectral techniques; IEE Proceedings E [see also Computers and Digital Techniques, IEE Proceedings-] Computers and Digital Techniques, Volume: 139 Issue: 4, Jul 1992, Page(s): 293 –307. Mahlstedt, U.; Alt, J.; Hollenbeck, I.; Deterministic test generation for non-classical faults on the gate level; Proceedings of the Fourth Asian Test Symposium, 23-24 Nov 1995, Page(s): 244 –251. Smith, D.T.; Johnson, B.W.; Profeta, J.A., III; System dependability evaluation via a fault list generation algorithm; IEEE Transactions on Computers, Volume: 45 Issue: 8, Aug 1996, Page(s): 974 –979.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph d. Torres, PhD
Art Unit 2133
May 20, 2003